GaAs MMIC PHASE LOCKED SOURCE

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ABSTRACT

A phase locked source has been designed, built and tested using a GaAs MMIC sampling phase detector and a GaAs MMIC VCO achieving phase lock up to 2 GHz with a 100 MHz input frequency.

INTRODUCTION

Phase locking an oscillator by utilizing a sampling phase detector (SPD) is a well known technique for achieving high frequency and low noise performance. Typically a sampling phase detector is built utilizing several components assembled onto a PC board or hybrid circuit as shown in Figure 1. The reference signal is amplified to about +27 dBm in the preamplifier to drive the step recovery diode (SRD). The SRD generates a comb of frequencies which goes into the input port of a balanced phase detector. The VCO is fed into the RF port of the phase detector. The IF port produces a low frequency signal proportional to the phase difference between the VCO frequency and the n^{th} harmonic of the SRD. The SPD can be modeled as a frequency multiplier cascaded to a phase detector as shown in Figure 2. The IF output will produce a signal whenever the VCO frequency coincides with a harmonic of the SRD comb.

The conventional sampling phase detector technology is unsurpassed in achieving high frequency performance because SRD's are efficient even beyond 30 GHz. This technique also results in wide loop bandwidths, low phase noise and low spurious noise because of the absence of frequency dividers. The main disadvantage to this technique is the circuit complexity, alignment time, parts count and power consumption which leads to the idea of producing it in MMIC form.

The VCO is a significant concern when designing a phase lock source. The phase noise, modulation sensitivity, and frequency stability of the VCO have a direct effect on the phase lock source performance. In order to achieve the desired loop performance in a repeatable manner the VCO must be tolerant to circuit variables which influence its characteristics. A MMIC VCO that includes on chip biasing, buffer amplifiers, and interstage matching makes a good PLL candidate because of its insensitivity to load pulling, frequency accuracy and repeatable modulation sensitivity.

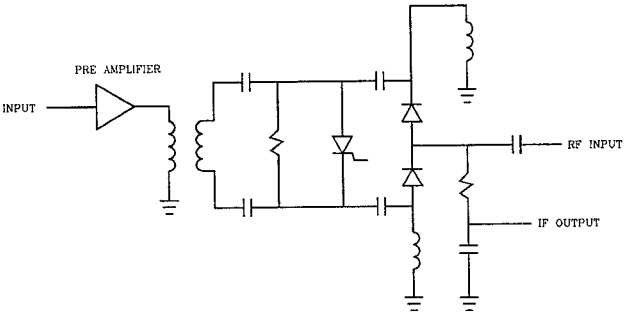

FIGURE 1 CONVENTIONAL SAMPLING PHASE DETECTOR CIRCUIT

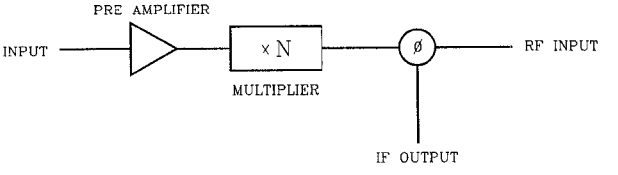

FIGURE 2 EQUIVALENT MODEL OF SAMPLING PHASE DETECTOR

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DESIGN THEORY

Much of the discrete SPD circuit can be integrated into MMIC form in order to reduce complexity and improve repeatability. A block diagram of the proposed circuit is shown in Figure 3. The preamplifier and SRD functions can be implemented onto the MMIC with FETs in a pulse forming network. The balanced phase detector can be put on the MMIC chip with a balanced pair of diodes. Good balance in the diodes is key to minimizing DC offsets which is critical in phase lock applications. Any DC offsets reduce the usable phase detector sensitivity. The MMIC approach is ideal for achieving good balance because the phase detector diodes process parameters are essentially identical and the input path lengths are fixed and repeatable unlike discrete diodes.

The VCO is a MMIC negative resistance chip which is described in reference 1. The remainder of the phase lock loop design is at video frequencies and is best implemented in discrete form. Silicon operational amplifiers are utilized for the loop filter and search circuit. A search circuit is necessary in an SPD PLL because there is no frequency acquisition capability in the phase detector once the VCO is beyond the locking range of the n^{th} comb signal. Silicon voltage regulators are used to establish stable biasing and minimize frequency pushing of the VCO.

EXPERIMENTAL RESULTS

MMIC Fabrication

The MMIC SPD was simulated on SPICE, laid out and fabricated as a 48x96 mil die as shown in Figure 4. The active devices are 100um FETS with .5 um gate lengths for the preamplifier and detector diodes. The FETs are actively biased in order to minimize the current consumption and improve the stability over temperature. On chip DC filtering and AC coupling is achieved with MIM capacitors. All bias points are on the MMIC chip so that the user need only provide one 5 volt bias.

Testing of MMIC SPD

The MMIC SPD was tested and exhibited good results. The input was fixed at 100 MHz at 5 dBm and the RF input was swept from 100 Mhz to 2 Ghz at -1 dBm. The MMIC was biased with 5 volts at 13 mA which is more than an order of magnitude less current than the conventional SPD. The IF output was monitored with an oscilloscope. The IF output measured less than 20 mV peak to peak across the band (less than 6 mV/radian) which is inadequate for phase locking purposes. The addition of another preamplifier cured the problem and provided a healthy 100 mV minimum peak to peak (33 mV/radian) which is adequate for phase locking. The additional preamplifier was built with silicon devices in hybrid form and consumes an additional 15 mA. The MMIC SPD can readily be revised to put another preamplifier on the MMIC circuit. The performance of the MMIC SPD with the bipolar preamplifier is shown in Table 1. The input can be driven at frequencies up to 500 Mhz and the RF port can be driven up to 2 Ghz. The DC offset is about 30 mV and does not vary significantly over temperature.

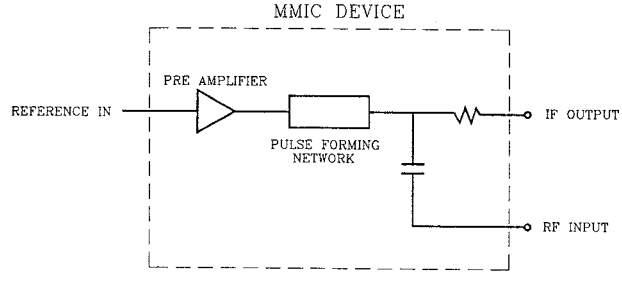

FIG 3. PROPOSED MMIC SAMPLING PHASE DETECTOR CIRCUIT

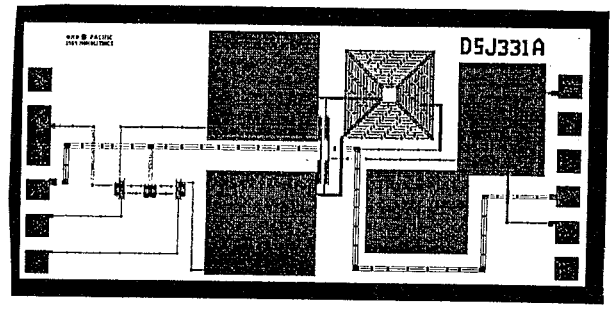

FIGURE 4. MMIC SPD DIE (48 x 96 MILS)

Table 1. Sensitivity Measurements of MMIC Sampling Phase Detector with Bipolar Preamplifier

Input reference = 100 MHz at 2 dBm
MMIC Bias = 5 V at 15 mA
Preamplifier Bias = 5 V at 14 mA
RF Input Power ~ 2 dBm

RF Input Frequency (Mhz)	IF Output Sensitivity (Volts Peak-Peak)
200 Mhz	270 mV
300	290
400	240
500	210
600	220
700	250
800	220
900	280
1000	270
1100	230
1200	230
1300	220
1400	200
1500	210
1600	200
1700	190
1800	140
1900	110
2000	100

Phase Lock Source Design

The phase lock loop was designed and built in hybrid form in a .5x.5 inch kovar flat pack as shown in Figure 5. The MMIC SPD and MMIC VCO are die attached to the package floor. The package contains Op amps for the search circuit and loop filter. Regulators are included in the package to maintain bias line stability. Tantalum capacitors are used to filter the bias lines. The preamplifier is a silicon integrated circuit. Chip capacitors and resistors are utilized for DC blocks and bias voltages. This circuit uses thin film circuitry as a prototype but can easily be designed in thick film to reduce the parts count and complexity.

Phase Lock Source Results

The MMIC phase locked source circuit was driven with a 100 MHz reference input from a crystal oscillator. The total power consumption of the phase locked source was 100 mA at 10 volts excluding the crystal oscillator. The MMIC VCO operates at 1.6 Ghz and has about 200 MHz/volt modulation sensitivity. The loop bandwidth was set at 400 KHz. A comparison of the VCO in the locked and unlocked condition is shown in Figure 6. The plot in Figure 7 illustrates the phase noise performance at 10 KHz offset which is less than -100 dBc/Hz. The free running MMIC VCO has a phase noise of about -67 dBc/Hz at 10 KHz which means that the loop is improving the phase noise by a factor of 33 dB. The plot in Figure 8 shows the spurious noise content. The 100 MHz spurs are about -75 dBc which is exceptionally good demonstrating that the small size of the circuit did not result in unacceptable crosstalk. The low spurious output is mainly due to the absence of frequency dividers which are notorious for spur contamination of the output.

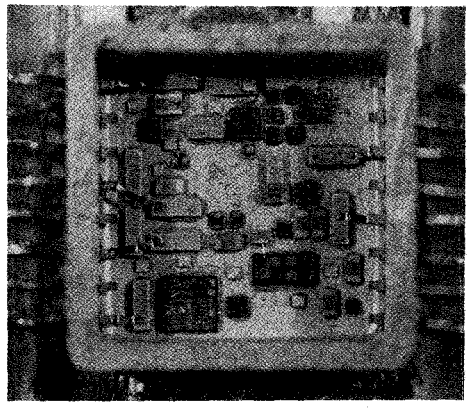

FIGURE 5. HYBRID MMIC SAMPLING PHASE DETECTOR PHASE LOCK SOURCE IN .5"x.5" FLAT PACK

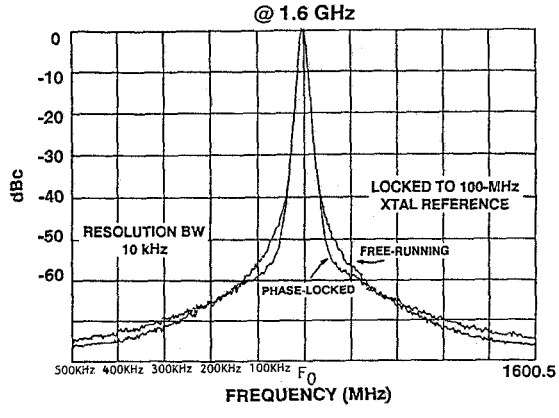

FIGURE 6. OUTPUT SPECTRUM OF MMIC SPD PLL IN LOCKED AND UNLOCKED CONDITIONS.

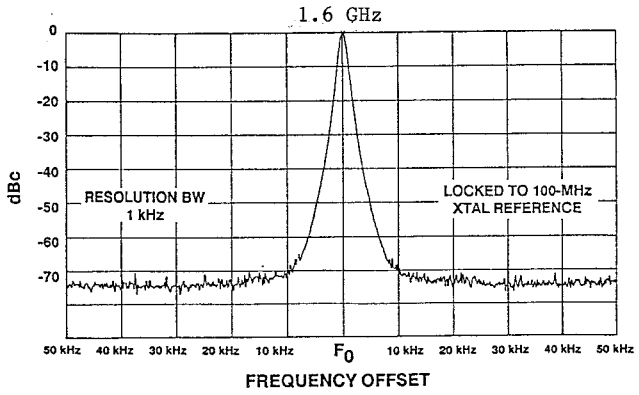

FIGURE 7. SPECTRAL PURITY OF MMIC SPD PLL AT 10 KHz OFFSET FREQUENCY

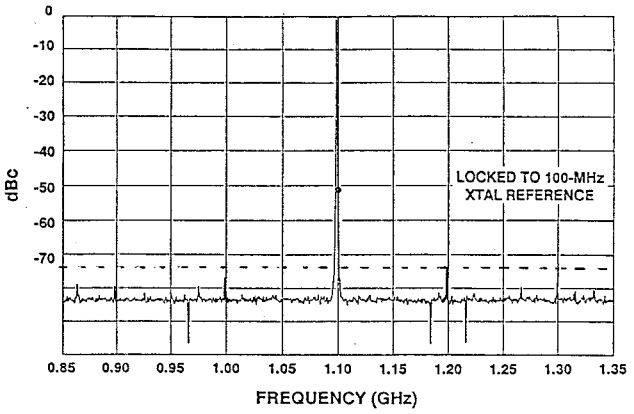

FIGURE 8. SPURIOUS OUTPUT SPECTRUM OF MMIC SPD PLL.

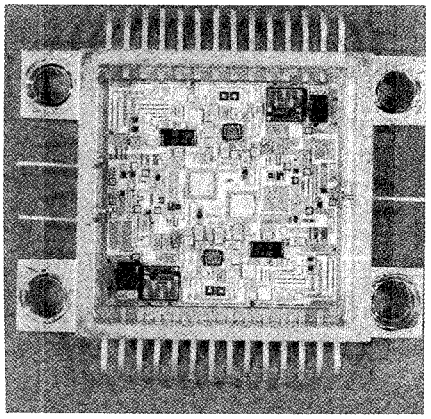

FIGURE 9. DUAL MMIC SAMPLING PHASE DETECTOR HYBRID PHASE LOCK SOURCE IN .8" x.8" INCH FLAT RACK.

Another PLL circuit was built using a bipolar VCO for a low phase noise application. A bipolar VCO has about 20 dB lower phase noise than a GaAs FET VCO. This design includes two hybrid PLL circuits in a .8x.8 inch flat pack as shown in Figure 9. One PLL is at 480 MHz and the other is at 840 Mhz and both are driven from a common 120 MHz crystal input. The total power consumption is less than 200 mA at 12 volts. The loop bandwidth is set at about 30 KHz. A phase noise plot is shown in Figure 10. The phase noise measures less than -110 dBc/Hz at 100 Hz which is exceptional for such a small, power efficient device.

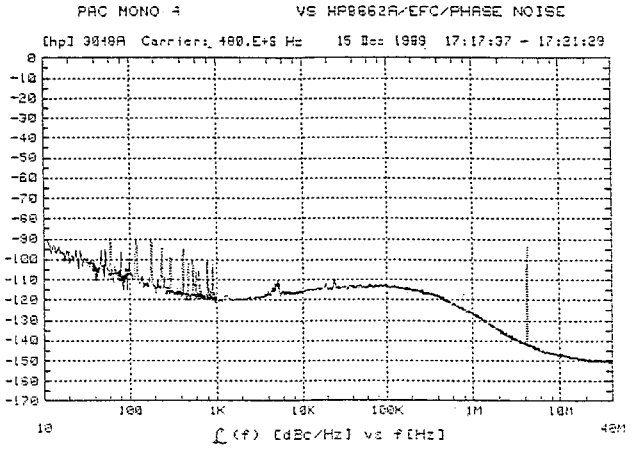

FIGURE 10. PHASE NOISE CHARACTERISTIC OF 480 MHz MMIC SPD PHASE LOCK SOURCE IN .8x.8 INCH FLATPACK.

CONCLUSION

A MMIC SPD was successfully designed, tested and integrated into a phase lock source. Phase lock source circuits were built and tested using both a MMIC and a bipolar VCO. The size, power consumption and noise performance are exceptional compared to conventional approaches.

REFERENCES

1. Sanjay B. Moghe and Thomas J. Holden, "High Performance MMIC Oscillators," IEEE MTTS, December 1987,pp. 1283-1287.